CLAIMS:

1. A method of trimming a gate electrode structure, the method comprising:

providing a gate electrode structure having a first dimension;

selecting a trimming recipe;

forming a reaction layer through reaction with the gate electrode structure; and

selectively removing the reaction layer from the unreacted portion of the gate electrode structure by chemical etching, thereby forming a trimmed gate electrode structure having a second dimension that is smaller than the first dimension.

2. The method according to claim 1, wherein the gate electrode structure comprises a gate electrode layer.

3. The method according to claim 2, wherein the gate electrode layer comprises at least one of a Si-containing layer and a metal-containing layer.

4. The method according to claim 3, wherein the gate electrode layer includes the Si-containing layer comprising amorphous Si, poly-Si, or SiGe.

5. The method according to claim 3, wherein the gate electrode layer includes the metal-containing layer comprising at least one of a metal, a metal nitride, or a metal oxide.

6. The method according to claim 3, wherein the gate electrode layer includes the metal-containing layer comprising at least one of TaN, TiN, TaSiN, Ru, and RuO_2.

7. The method according to claim 2, wherein the gate electrode structure further comprises an ARC layer.

8. The method according to claim 7, wherein the ARC layer comprises an organic ARC layer or an inorganic ARC layer.

9. The method according to claim 7, wherein the ARC layer comprises SiN.

10. The method according to claim 1, wherein the forming comprises exposing the gate electrode structure to a reactant gas in a thermal process or in a plasma process.

11. The method according to claim 1, wherein the reaction layer is formed in a self-limiting process.

12. The method according to claim 10, wherein the reactant gas comprises an excited oxygen-containing gas.

13. The method according to claim 1, wherein the forming comprises exposing the gate electrode structure to a wet oxidation process.

14. The method according to claim 1, wherein the removing comprises exposing the gate electrode structure to an etch gas.

15. The method according to claim 1, wherein the removing comprises exposing the gate electrode structure to $HF_{(aq)}$.

16. The method according to claim 1, wherein the removing comprises exposing the gate electrode structure to HF and NH_3 gases and then to a heat treatment.

17. The method according to claim 1, wherein the removing comprises exposing the gate electrode structure to NF_3 and NH_3 gases in a remote plasma and then to a heat treatment.

18. The method according to claim 1, wherein the removing comprises exposing the gate electrode structure to a wet process.

19. The method according to claim 1, wherein the exposing and removing are carried out in a single processing system.

20. The method according to claim 1, wherein the forming and removing are carried out in multiple processing systems.

21. The method according to claim 1, wherein the first dimension is a lithographic dimension.

22. The method according to claim 1, further comprising measuring at least one of the first and second dimensions of the gate electrode structure.

23. The method according to claim 1, further comprising repeating the selecting, forming, and selectively removing at least once.

24. The method according to claim 1, further comprising using the trimmed gate electrode layer as a mask layer for anisotropic etching.

25. The method according to claim 1, wherein the forming includes forming an oxide layer on a surface of the gate electrode.

26. A computer readable medium containing program instructions for execution on a processor, which when executed by the processor, cause a processing tool to perform the steps of claim 1.

27. A semiconductor device, comprising:

a trimmed gate electrode structure formed by the method of claim 1.

28. A processing tool, comprising:

a substrate loading chamber configured for loading and unloading a substrate with a gate electrode structure having a first dimension;

a transfer system configured for transferring the substrate within the processing tool;

at least one processing system configured for forming a reaction layer through reaction with the gate electrode structure and selectively removing the reaction layer from the unreacted portion of the gate electrode structure by chemical etching; and

a controller configured for controlling the processing tool according to a trimming recipe to form a gate electrode structure having a second dimension that is smaller than the first dimension.

29.The processing tool according to claim 28, wherein the forming comprises exposing the gate electrode structure to a reactant gas in a thermal process or in a plasma process.

30.The processing tool according to claim 28, wherein the removing comprises exposing the gate electrode structure to an etch gas.

31.The processing tool according to claim 28, further comprising a further processing system configured for plasma etching.

32.The processing tool according to claim 31, wherein the further processing system is configured for RIE.

33.The processing tool according to claim 28, wherein the at least one processing system is configured for wet processing.

34.The processing tool according to claim 28, further comprising a processing system configured for measuring at least one of the first and second dimensions of the gate electrode layer.